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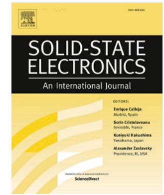

Low-frequency noise characterization of positive bias stress effect on the spatial distribution of trap in β-Ga_2O_3 FinFET

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ABSTRACT

The reliability of a β-Ga_2O_3 thin-film field-effect transistor is investigated under positive-bias stress (PBS). The transistor has a tri-gate structure with a gate dielectric of Al_2O_3. By characterizing low-frequency noise (LFN), the spatial distribution of trap in the gate dielectric was quantitatively extracted. The measured power spectral density (PSD) followed a 1/f-shape due to trapping and de-trapping of the channel carriers to and from the gate dielectric. Notably, the vertical distribution of the traps perpendicular to the interface of β-Ga_2O_3 and Al_2O_3 was mapped

1. Introduction

Beta-gallium oxide (β-Ga_2O_3) is a promising candidate for next generation power devices due to its wide energy bandgap (E_G) of 4.8 eV and high breakdown electric field (E_{BD}) of 8 MV/cm compared with SiC and GaN materials [1–6]. Unlike the conventional Schottky gate structures, *i.e.*, GaN high-electron mobility transistors (HEMTs), the instability of a gate dielectric on a β-Ga_2O_3 channel, which is related to traps in the gate dielectric, can be an obstacle to achieving high E_{BD} and suppressing gate leakage current (I_G). Extraction of the dielectric traps is thus important for long-term and reliable operations. Thus far, several meaningful investigations of the reliability issues in β-Ga_2O_3 FETs have been reported [7–10]. When the temperature of β-Ga_2O_3 FET was increased, off-state current (I_{off}) and sub-threshold slope (*SS*) increased, and on-state current (I_{on}) decreased compared to before the room temperature (RT) by analyzing the transfer curve characterization [3]. However, a quantitative investigation of the spatial distribution of oxide and interface traps in the gate dielectric of the β-Ga_2O_3 FETs has not been reported yet. Meanwhile, an analysis of low-frequency noise (LFN) is a powerful characterization technique for studying the carrier transport properties and evaluating the quality of gate dielectrics [11–17]. Furthermore, the LFN analysis is applicable even to a MOSFET with a floating body, because it characterizes the drain current (I_{DS}) rather than the body current (I_B). Unlike the conventional charge pumping technique to extract traps near the interface of the gate dielectric-to-channel via the I_B, the LFN technique is advantageous to profile the spatial distribution of traps (N_T) inside the bulk of the gate dielectric [18,19]. This work quantitatively investigated the spatial distribution of N_T in a β-Ga_2O_3 FET with a tri-gate structure and a gate dielectric of Al_2O_3. The nominal dimensions of the fabricated β-Ga_2O_3 FET are a channel width (W_{CH}) of 50 nm, a gate length (L_G) of 1 µm, and a channel height (H_{CH}) of 100 nm. The vertical distribution of the N_T perpendicular to the interface of the β-Ga_2O_3-to-Al_2O_3 was profiled for various V_G through the LFN and DC I-V. The cases before and after positive-bias stress (PBS) were then compared. Whereas the N_T prior to the PBS was uniformly distributed, that after the PBS was spatially varied.

2. Device fabrication and measurement

For the fabrication of the tri-gate β-Ga_2O_3 FETs, a thin (1 0 0) β-Ga_2O_3 nano-membrane doped by Sn with a doping concentration of 2.7 × 10^{18} cm^{-3} was transferred from the bulk β-Ga_2O_3 substrate onto a p^+ Si wafer

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with a 270 nm thick SiO_2 layer. It was delineated by a 1st electron beam (e-beam) lithography step and patterned by subsequent dry-etching for a channel [20,21]. Afterwards, the source (S) and the drain (D) regions were defined by following three steps: 2nd e-beam lithography, metal deposition, and a lift-off process. For the S/D metals, Ti, Al, and Au, were sequentially deposited with respective thickness of 15 nm, 60 nm, and 50 nm. Thereafter, Al_2O_3 was deposited by atomic layer deposition (ALD) for a gate dielectric. Lastly, Ni and Au with a thickness of 50 nm and 80 nm, respectively, were deposited by an e-beam evaporator and patterned by a 3rd e-beam lithography step and etching for a gate electrode, as shown in Fig. 1. Fig. 1(a) shows a schematic illustration of the tri-gate β-Ga_2O_3 FET. To demonstrate the narrow tri-gate channel clearly, a SEM image of the fabricated device before gate metal deposition is provided in Fig. 1(b). The LFN measurement obtained RTS noise through a low-noise current preamplifier (SR570) by applying DC bias to the gate and drain with a parameter analyzer (4155B). Next, 1/f noise was measured through the vector-signal analyzer (89410A) to convert RTS noise from the following time domain to the frequency domain.

3. Low-frequency noise characterization

Fig. 2 illustrates the depth profile of trap along the vertical direction in the Al_2O_3/β-Ga_2O_3 gate stack obtained by using LFN measurement. The LFN includes thermal noise, which is the random thermal motion of electrons. The power spectral density (PSD) of the thermal noise current is given as follows (1):

$$S_{ID} = \frac{4kT}{R} \tag{1}$$

where T is temperature, k is Boltzmann's constant, and R is the resistance [11]. The PSD follows a $1/f$-shape, which is caused by the trapping and de-trapping of channel charges to and from the traps in the gate dielectric. Therefore, the vertically spatial distribution of traps can be quantitatively mapped and the depth profile before and after the bias stress can be compared. The carrier number fluctuation (CNF) correlated with carrier mobility fluctuation (CMF) is one of the mechanisms of the LFN. It is based on the interaction between traps in a gate dielectric and carriers in the channel [11]. The noise signal is mainly attributed to the trapping/de-trapping events caused by the tunneling of charge carriers into and from the traps, which are located near the interface of the gate dielectric and channel. The normalized PSD of drain current (S_{ID}/I_D^2) according to the CNF and CMF model is expressed as follow (2):

$$\frac{S_{ID}}{I_D^2} = \left(1 + \alpha_{sc}\mu_{eff}C_{ox}\frac{I_D}{g_m}\right)^2 \left(\frac{g_m}{I_D}\right)^2 SVFB, \tag{2}$$

where α_{sc} is the Coulomb scattering coefficient, g_m is the transconductance (defined as $\partial I_D/\partial V_G$) [11]. S_{VFB} is the flat-band voltage noise PSD is given as follows (3):

$$S_{VFB} = \frac{q^2 kT\lambda N_T}{WLC_{ox}^2 f} \tag{3}$$

where N_T is the trap density and λ is the tunneling attenuation length in the gate dielectric (0.1 nm for Al_2O_3) [11].

The gate voltage noise spectrum can calculate the physical distance dependence of the N_T from the frequency f, which is expressed as follows (4):

$$x = \lambda \ln\left(\frac{1}{2\pi f\tau_0}\right) \tag{4}$$

where τ_0 is the characteristic time constant, which is usually taken as 10^{-10} sec [11]. Note that τ is the tunneling time constant and is defined as $1/2\pi f$. τ is determined by the physical distance (x) of a trap perpendicular to the β-Ga_2O_3/Al_2O_3 interface. Because the PSD of referred-input gate voltage noise (S_{VG}) is defined as S_{ID}/g_m^2, N_T can be extracted from the frequency-dependent S_{VG}.

4. Experimental results

Fig. 3(a) and (b) show the measured I_D-V_G and I_D-V_D characteristics from the fabricated β-Ga_2O_3 FET. The characteristics before and after the PBS were compared. The detailed PBS conditions are V_G of 4.5 V, $V_D = V_S$ = ground and stress time of 1000 sec. Such PBS induces N_T in the Al_2O_3 gate dielectric. It interacts with the channel carriers, provokes mobility degradation, and results in decreasing I_{ON}. On the other hand, N_T causes additional parasitic capacitance, degrades the *SS,* and shifts the threshold voltage (V_T). As a consequence, three representative device parameters, I_{ON}, *SS*, and V_T, were degraded by the PBS, as shown in Fig. 3.

In order to quantitatively extract N_T, LFN analyses were conducted. As shown in Fig. 4(a) and (b), the PSD was measured at the initial state and after PBS damage [22]. A normalized value of drain-current PSD follows a $1/f$-shape in a frequency range of 10 Hz to 1610 Hz. The V_T is extracted via linear extrapolation method and was negatively shifted from the initial data to 2.3 V and to 1.5 V after PBS. At $V_G = V_T + 2$ V, the level of the PSD with PBS is two orders higher than that without PBS. It is important to evaluate how well the measured data correlate with the noise model prior to the LFN characterization. The normalized PSD values multiplied by frequency and g_m^2/I_D^2 were overlaid as a function of I_D before and after PBS at 10, 100, and 1000 Hz, as shown in Fig. 5 (a) and (b). In the weak inversion region, the normalized PSD values are well correlated with the g_m^2/I_D^2 values, verifying that the noises can be ascribed to the CNF. In the strong inversion region, the parasitic resistance effect (R_{SD}) arising from the source and drain contacts becomes larger [23]. Therefore, the normalized PSD values at higher I_D deviate from the g_m^2/I_D^2 values. N_T values along with the vertical depth direction were extracted from the measured PSD values, as shown in Fig. 6. The level of N_T after PBS is always above that before PBS (initial) regardless

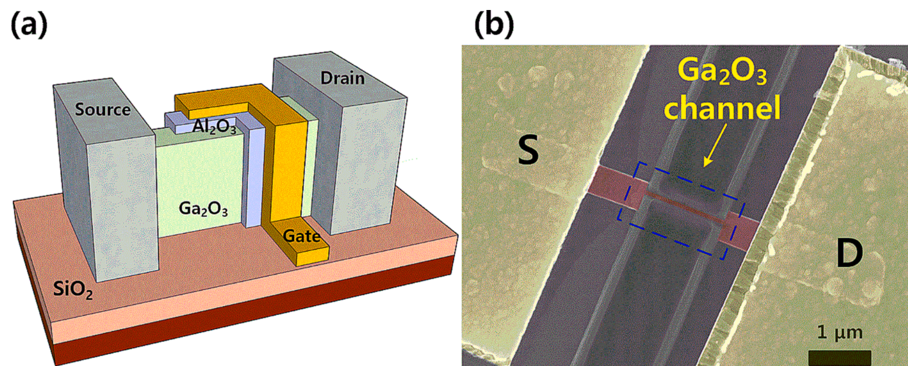

Fig. 1. (a) Cross-sectional schematic along the channel width direction. (b) SEM image of the fabricated device after RIE etching.

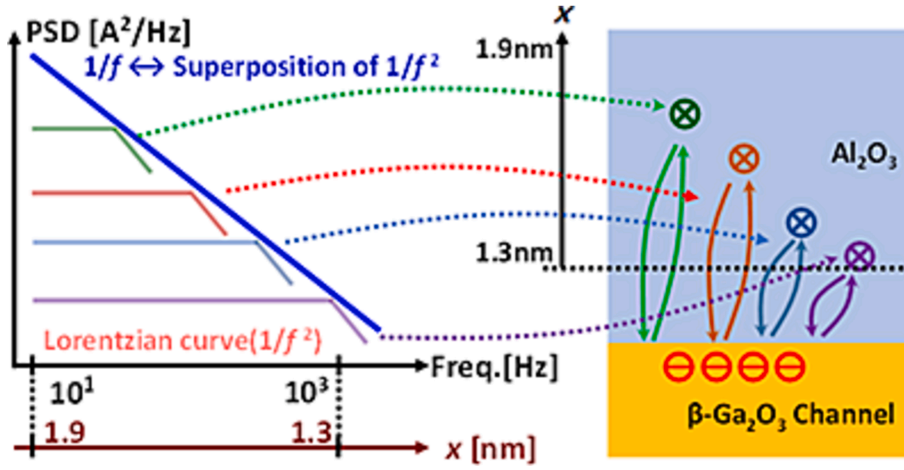

Fig. 2. Cross-sectional view of a gate stack and PSD for varied f and its corresponding x, which is the distance from the interface and is extracted from Equation (2) as a function of f.

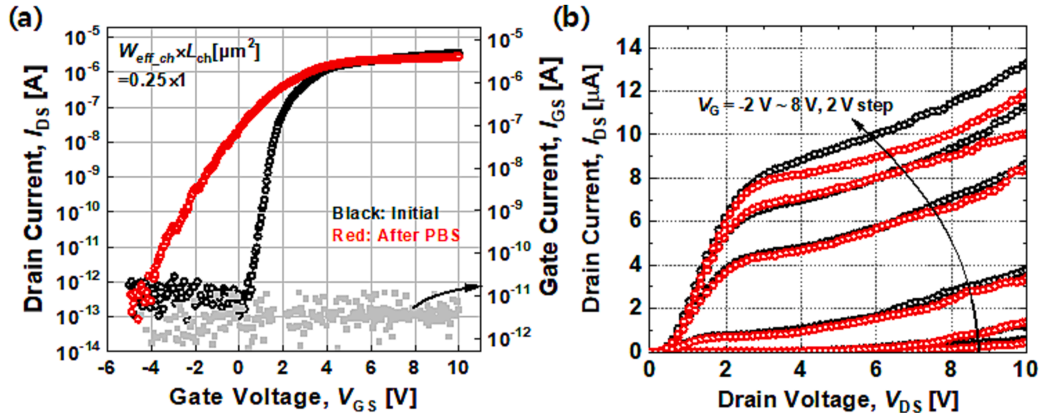

Fig. 3. Measured characteristics from the fabricated β-Ga_2O_3 FETs. (a) Comparison of I_{DS}-V_{GS} with and without PBS. (b) Compared I_{DS}-V_{DS} for with and without PBS.

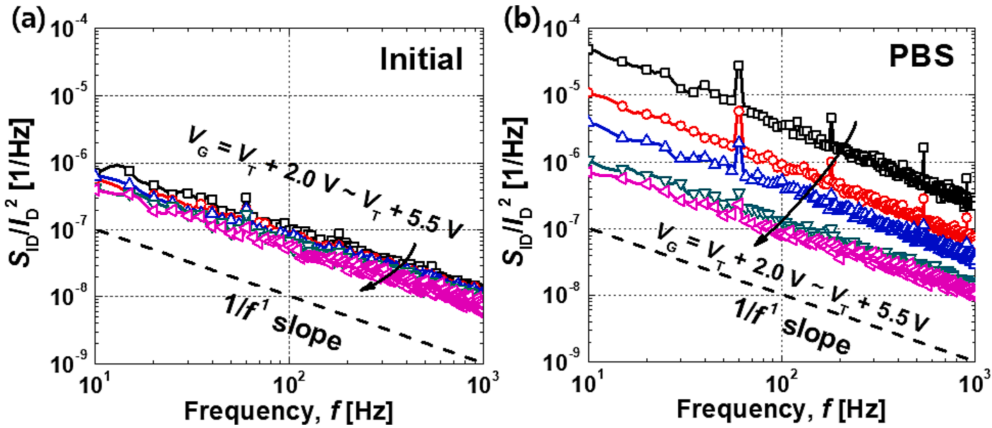

Fig. 4. Normalized drain-current PSD (S_{ID}/I_D^2) as a function of f: (a) Initial state and (b) after PBS.

of the depth position (x). In particular, the amount of traps increases with a deeper x. This implies that injected carriers gain higher energy by PBS as x becomes farther from the interface. The extracted oxide trap and interface trap (D_{it}) [8] densities before and after PBS is summarized in Table 1.

5. Conclusion

The spatial trap distribution (N_T) in an Al_2O_3 gate dielectric of a β-Ga_2O_3 FET with a 3-D tri-gate structure was characterized along the depth direction by analyzing the measured characteristics of low-frequency noise (LFN). It was confirmed that N_T was increased by positive-bias stress (PBS) and became non-uniformly distributed. The incremental tendency of N_T with a deeper position in the Al_2O_3 arises

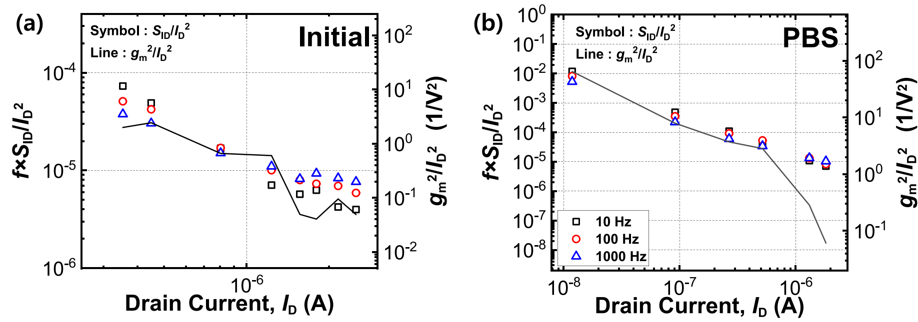

Fig. 5. Normalized drain-current noise PSD multiplied by frequency ($f \times S_{ID}/I_D^2$; symbols) at 10 Hz and (g_m^2/I_{DS}^2; solid line) as a function of drain-current (I_D): (a) Initial state and (b) after PBS.

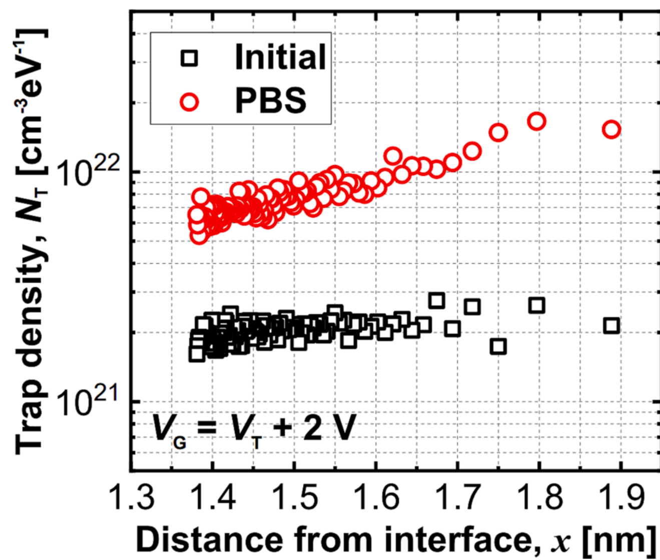

Fig. 6. Comparison of extracted trap density from PSD values between initial state and after PBS under $V_G = V_T + 2$ V (Strong inversion region).

Table 1
Extracted Trap Density before and after PBS.

	N_T [cm^{-3}eV^{-1}]	D_{it} [cm^{-2}eV^{-1}]
before PBS	~2×10^{21}	~8×10^{11}
after PBS	~2×10^{22}	~7×10^{12}

from higher stress voltage applied to the gate. This work can pave the way to advance devices based on a β-Ga_2O_3 channel via characterizing N_T to explore optimal gate dielectrics.

CRediT authorship contribution statement

Hagyoul Bae: Conceptualization, Data curation, Formal analysis, Funding acquisition, Investigation, Methodology, Resources, Supervision, Visualization, Writing – original draft, Writing – review & editing. **Geon Bum Lee:** Investigation, Formal analysis, Writing – original draft, Writing – review & editing. **Jaewook Yoo:** Investigation, Visualization, Writing – review & editing. **Khwang-Sun Lee:** Formal analysis, Methodology. **Ja-Yun Ku:** Formal analysis, Investigation, Methodology. **Kihyun Kim:** Formal analysis, Resources. **Jungsik Kim:** Investigation, Software. **Peide D. Ye:** Investigation, Methodology, Supervision. **Jun-Young Park:** Data curation, Investigation, Writing – original draft. **Yang-Kyu Choi:** Formal analysis, Investigation, Supervision, Validation, Writing – original draft.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

No data was used for the research described in the article.

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